Area-Efficient and Low-Power Decimation Filter for VLSI Integration

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***Abstract*—This paper addresses the design of a decimation filter for VLSI integration, with a focus on minimizing both silicon area and power consumption. A CIC filter-based architecture, employing an IIR-FIR structure, is utilized to achieve this goal. The paper outlines the design process, from system-level modeling to hardware synthesis and layout. The resulting design offers a competitive solution for applications where power efficiency and compact size are critical design constraints.**

I. Introduction

Analog filters typically offer cost-efficiency, rapid response, and extensive dynamic range across amplitude and frequency domains. Conversely, digital filters provide markedly enhanced performance capabilities unattainable by their analog counterparts. The superiority in precision and quality that digital filters exhibit stems from fundamentally distinct approaches to the filtering challenge.

In analog implementations, components such as resistors and capacitors impose intrinsic constraints on accuracy and stability. Digital filters, by contrast, prioritize signal constraints and theoretical processing methodologies to optimize filter behavior. The performance of digital signal processing and communication frameworks is predominantly constrained by the input signal's fidelity.

The escalating adoption of digital telecommunication technologies, especially in audio processing, has driven the widespread utilization of analog-to-digital converters. Nonetheless, traditional converter architectures struggle to achieve high-performance metrics within compact physical dimensions. Ongoing advancements in telecommunication technologies surpass these limitations, facilitating future system improvements including enhanced integration density, reduced power consumption, smaller device footprints, and the capability to support a greater number of simultaneous communication channels.

Signal transmission frequently employs modulation techniques such as coded pulse modulation, with digital filtering constituting a fundamental operation. Filtering is extensively utilized in electronic systems to suppress unwanted or corrupted signal components. In the time domain, digital filters are characterized by difference equations, whereas transfer functions represent them in the frequency domain.

Two primary categories of digital filters exist: Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters. Both filter types have distinct strengths and weaknesses summarized in Table I.

TABLE I
Comparative Analysis of Digital Filter Types

Filter Type	Benefits	Limitations
FIR	leftmargin=*, noitemsep, topsep=0pt • Linear phase • Stable behavior • Low quantization noise • Simple to implement	High order required
IIR	leftmargin=*, noitemsep, topsep=0pt • Low order filter • Possible instability	leftmargin=*, noitemsep, topsep=0pt • Complex design • Limit cycles risk

A notable drawback of FIR filters is their higher order relative to IIR filters that exhibit comparable frequency responses. Consequently, FIR implementations incur increased size, power demands, and computational overhead. An effective approach to mitigate this challenge is the use of Interpolated FIR (IFIR) filters, which considerably diminish the filter order. The architecture of IFIR filters is detailed in subsequent sections.

This manuscript is structured as follows: an initial discussion on decimation filters integrating FIR and IIR components, followed by an exposition of Cascaded Integrator Comb (CIC) and Half-Band filters, including MATLAB-based behavioral simulations. Subsequently, the synthesis of the decimation filter is presented, highlighting the extraction of standard cell netlists from Verilog descriptions to generate integrated circuit layouts via Cadence tools. Finally, performance parameters of the decimation filter are compared against prevalent designs.

II. Decimation Filter

Decimation filters are fundamental components in digital signal processing systems, especially in applications involving oversampled data such as sigma-delta analog-to-digital converters (ADCs). These filters combine both Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) structures to efficiently reduce the sampling rate of a signal by an integer factor M, which is commonly referred to as the decimation factor or oversampling ratio. The main objective of a decimation filter is to eliminate out-of-band noise and spectral components that lie outside the desired frequency band, thereby preventing aliasing during the downsampling process.

The operation of a decimation filter is critical in converting a high-rate, coarsely quantized digital signal—often the output

of a sigma-delta modulator—into a lower-rate, high-resolution digital representation. The filter works by averaging or integrating M samples from the modulator's output, effectively smoothing the signal and reducing noise. This process enhances the signal-to-noise ratio (SNR) and produces a cleaner, lower-frequency digital output suitable for further processing or analysis.

Mathematically, the relationship between the output sampling frequency F_s and the input sampling frequency F_e is given by the ratio

$$\frac{F_s}{F_e} = \frac{1}{M}$$

where M is the integer decimation factor. Consequently, the decimation filter must be designed to isolate and preserve the frequency content within the band $[0, F_s/2]$, which corresponds to the Nyquist band of the downsampled signal. The filter must effectively suppress spectral components above this band to prevent aliasing when the signal is downsampled by a factor of M.

One of the crucial design considerations in decimation filtering is the preservation of signal integrity within the passband. This requires the filter to maintain a linear phase response to avoid phase distortion, which can adversely affect signal characteristics such as timing and waveform shape. FIR filters are particularly favored in this context due to their inherent linear phase properties, although their implementation can be resource-intensive. IIR filters, on the other hand, offer computational efficiency but typically exhibit nonlinear phase responses, requiring careful design to mitigate distortions.

Given the potentially high computational cost of implementing a single-stage decimation filter—especially for large decimation factors and stringent stopband attenuation requirements—multistage decimation is widely adopted as an effective strategy. Multistage decimation involves cascading several filters, each performing decimation by a smaller factor, such that the overall decimation factor is the product of the individual stage factors. This approach significantly reduces the filter complexity by spreading the decimation process over multiple stages and progressively lowering the sampling rate at each step.

For instance, an initial stage might employ a simple, computationally light filter such as a comb filter to reduce the sampling rate by a moderate factor. Subsequent stages use more sophisticated filters with narrower transition bands to refine the signal quality further. This hierarchical approach minimizes the total number of filter taps required, which directly impacts the computational load and power consumption.

It is also important to note that the number of filter taps in an FIR decimation filter is proportional to the required stopband attenuation and inversely proportional to the transition bandwidth between the passband and stopband. A narrow transition band or high stopband attenuation demands a longer filter, increasing hardware complexity and power consumption. By breaking the decimation into multiple stages, the filters at each stage can operate with relaxed specifications, reducing the overall system complexity.

In addition to reducing computational load, multistage decimation offers significant power savings, which is crucial in battery-powered and low-power embedded systems. Since power consumption scales with both the number of filter taps and the operating frequency, reducing the sampling frequency after each stage allows the subsequent filters to operate at lower clock rates, thereby decreasing dynamic power dissipation.

In summary, decimation filters play an essential role in digital signal processing by enabling efficient sampling rate reduction while preserving signal fidelity. The combined use of FIR and IIR structures, together with multistage filtering architectures, provides a flexible and powerful design framework to balance performance, complexity, and power consumption. Understanding these design trade-offs is key to developing optimized decimation filters tailored to the requirements of modern high-performance digital communication and measurement systems.

III. Cascaded Integrator-Comb (CIC) Filter

Various architectures for decimation filters exist, including polyphase, hybrid IIR-FIR, and non-recursive configurations. Polyphase designs typically demand extensive silicon area but offer low power usage, whereas hybrid IIR-FIR structures tend to consume more power with reduced chip area requirements.

This study adopts a hardware-based multistage decimation filter utilizing a Cascaded Integrator-Comb (CIC) structure, as illustrated in Fig. 1. The IIR section functions as an integrator operating at the input sampling frequency F_s, while the FIR section serves as a differentiator working at the decimated rate F_s/M.

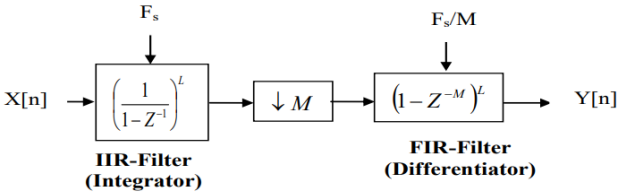

Fig. 1. Block Diagram of CIC Decimation Filter Employing IIR-FIR Architecture

The CIC filter transfer function can be expressed as:

$$H(z) = \left(\frac{1 - z^{-M}}{1 - z^{-1}}\right)^{L} \tag{1}$$

where M denotes the oversampling ratio, and L represents the filter order. The numerator $(1 - z^{-M})^L$ corresponds to the differentiator stage, whereas the denominator $(1 - z^{-1})^L$ models the integrator component. The overall decimation filter comprises multiple cascaded stages.

A. Half-Band Filter Design

Half-band filters constitute a specialized FIR filter category optimized for decimation by a factor of two. This filter is typically realized by cascading two FIR filters, each performing downsampling by 2. The initial FIR stage compensates for distortion introduced by preceding sinc blocks, acting as a low-pass filter with noise shaping beyond its passband. The final FIR stage provides sharp frequency selectivity.

The coefficients of the FIR filters leverage Canonical Signed Digit (CSD) representation, facilitating hardware implementation with reduced complexity. CSD encoding minimizes the number of nonzero digits compared to binary representations, leading to fewer add-and-shift operations and enhanced tolerance to coefficient quantization.

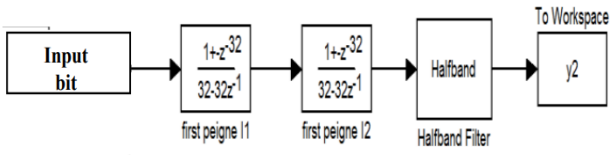

Fig. 2. MATLAB Simulation Model of the Half-Band Filter

The combination of the CIC filter as the initial stage followed by the half-band filter achieves the downsampling to the Nyquist frequency, as depicted in Fig. 2.

B. Design and Simulation Approach

The design goal encompasses a multistage decimation filter, with intermediate stages tailored for relaxed specifications to optimize resource usage. The initial stage is partitioned into two subsystems with complementary objectives to be discussed in further detail.

Decimation is performed in two sequential stages: initially by a factor of 8, followed by a factor of 4, aiming to reduce the order of the sinc filter. The first stage employs a fourth-order filter, whereas the subsequent stage utilizes a third-order filter. This partitioning strategy effectively lowers the overall filter orders and thus diminishes their complexity. The final half-band filter adheres to stringent performance requirements, while the initial half-band filter accommodates a comparatively wider transition bandwidth.

Simulation executed via MATLAB yielded the frequency response characteristics illustrated in Fig. 3, depicting the magnitude response of the cascaded sinc filter stages.

Fig. 4 presents the overlay of the sinc filter amplitude attenuation curve alongside the ideal FIR filter frequency response following the first half-band filter stage.

Subsequently, Fig. 5 illustrates the normalized and composite frequency response after the second half-band filter (HB2), representing the complete output of the decimation sequence.

C. Filter Synthesis

The synthesis workflow, summarized in Fig. 6, involved extraction of the standard cell netlist from the Verilog description, which was subsequently imported into a VHDL

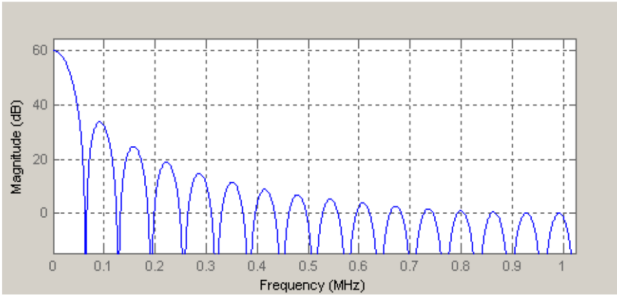

Fig. 3. Frequency response of the cascaded sinc filter stages

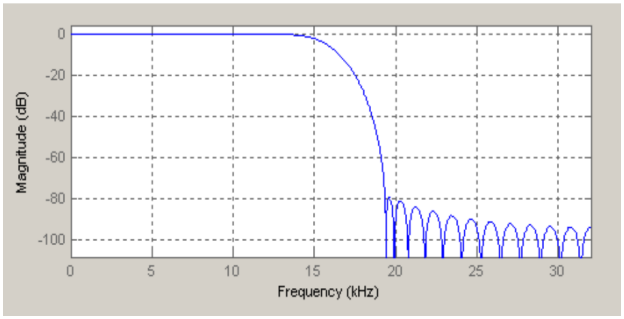

Fig. 4. Normalized and combined frequency response after first half-band filter (HB1)

simulator for preliminary verification. Logical verification was performed using Cadence NCsim, employing the original testbench to ensure functional equivalence.

The simulation outputs, digital samples from filter responses, were processed in MATLAB with Fast Fourier Transform (FFT) analysis to validate the frequency-domain characteristics. Successful verification confirmed compliance with design criteria. Physical design stages, including floorplanning, placement, routing, and clock/reset tree synthesis, were conducted using Cadence Silicon Ensemble. The final Verilog netlist was re-simulated with NCsim to perform a comprehensive verification of the digital subsystem.

D. Filter Layout

Following netlist extraction, physical design proceeded to generate the integrated circuit layout. This phase converts circuit components and interconnects into a geometric representation compatible with fabrication requirements. Fig. 7 displays the resulting layout of the decimator filter.

Table II compares this work against prominent previously published designs, highlighting significant improvements. Notably, the proposed design demonstrates lower power consumption at 2.94 mW and reduced silicon area of 0.058 mm^2. Furthermore, the design attains a higher operational frequency of 10.24 MHz.

IV. Conclusion

The implementation and verification of a multi-stage decimation filter chain have been successfully completed, demonstrating the effectiveness of a hierarchical filtering approach

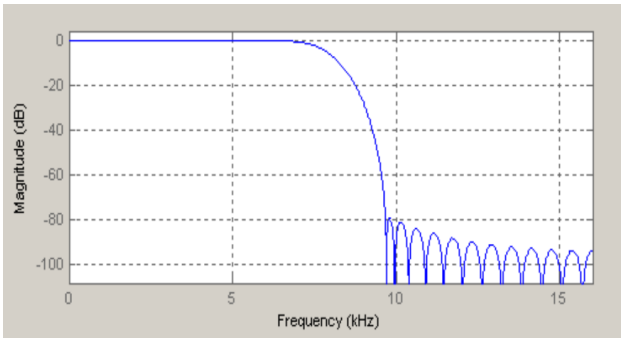

Fig. 5. Normalized and combined frequency response after second half-band filter (HB2)

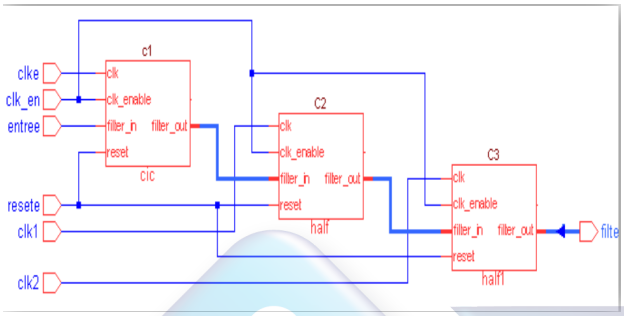

Fig. 6. Filter synthesis process flow

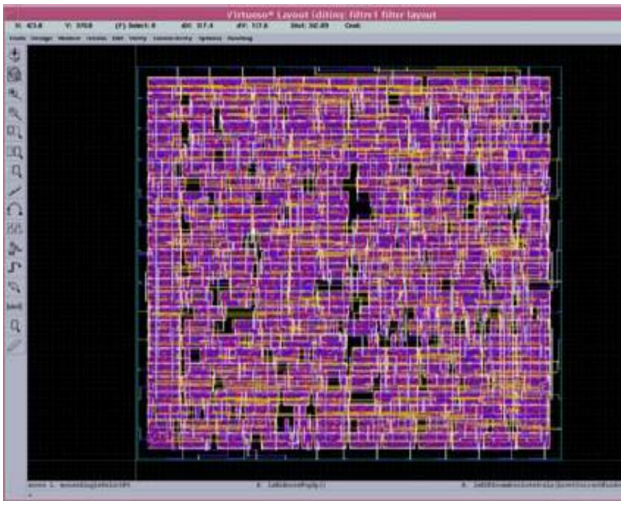

Fig. 7. Layout of the decimation filter

TABLE II
COMPARISON OF NOTABLE FILTER IMPLEMENTATIONS

Design	Power (mW)	Area (mm^2)	Max Frequency (MHz)
Prior Work 1	4.1	0.10	8.5
Prior Work 2	3.5	0.08	9.2
Current Work	**2.94**	**0.058**	**10.24**

in achieving efficient sampling rate reduction for oversampled digital signals. This work highlights the practical advantages of employing a staged architecture, combining multiple filtering blocks—each tailored for specific frequency ranges and sampling rates—thereby reducing the overall computational complexity and hardware resource requirements of the decimation process.

Verification and simulation were carried out within the Cadence standard verification environment, a robust and industry-accepted tool suite for ASIC and mixed-signal design validation. These results confirmed the functional correctness and robustness of the filter design under a variety of input conditions and operating scenarios. The validation ensures that the proposed architecture maintains signal integrity, avoids aliasing, and meets the necessary spectral constraints, rendering it suitable for use in real-world applications where power efficiency, area constraints, and computational limitations are critical considerations.

The proposed decimation filter chain is composed of several well-structured stages, each contributing to the progressive reduction of the sampling rate. The first and second stages consist of sinc (Cascaded Integrator-Comb) filters, which perform decimation by factors of 8 and 4, respectively. These filters are particularly effective for handling high initial oversampling rates with minimal resource overhead due to their multiplier-free structure. Following the sinc filters, two half-band filters—each responsible for a further decimation by a factor of 2—are used to refine the spectral characteristics of the signal. These half-band filters ensure sharp transition bands and excellent alias suppression, making them ideal for the final stages of decimation where higher fidelity is demanded.

One of the standout features of the proposed architecture is its inherent platform independence. This allows the design to be ported and deployed across various FPGA platforms with minimal customization, thereby enhancing its versatility and practical applicability in a wide range of signal processing tasks. Such flexibility is highly beneficial for prototyping and iterative design in rapidly evolving embedded system environments.

From a physical implementation perspective, the decimation filter was fabricated using AMS 0.35 μm CMOS technology. The fabricated Cascaded Integrator-Comb (CIC) filter, forming the backbone of the initial decimation stages, was tested under a 3V power supply and exhibited a remarkably low power consumption of only 2.94 mW. This low-power profile makes the filter chain particularly attractive for battery-powered and energy-sensitive applications, such as biomedical signal acquisition, portable instrumentation, and wireless communication systems.

Looking forward, several avenues for future research and development have been identified. One promising direction is the integration of additional analog-to-digital converter components—most notably, the sigma-delta modulator block—to develop a fully integrated and self-contained ADC solution. This would facilitate a comprehensive design and testing pipeline for next-generation ADCs, enabling tighter coupling between the modulator and decimation stages, which can lead to enhanced performance and power savings.

Another important research direction involves the explo-

ration of multi-bit discrete-time sigma-delta ADC architectures. These architectures offer improved resolution and dynamic range but pose new challenges in terms of digital decimation filter design, particularly in handling increased quantization noise and maintaining linearity. The development of efficient and scalable filter designs compatible with multi-bit quantization is therefore a key area of interest.

In parallel, ongoing efforts will focus on the physical fabrication and experimental validation of the proposed decimation filter. Detailed measurement and characterization of performance metrics—such as frequency response, stopband attenuation, in-band ripple, group delay, and total harmonic distortion (THD)—will be conducted to verify that the implementation meets theoretical predictions and design specifications. Such empirical results will further substantiate the suitability of the design for deployment in commercial or industrial applications.

In conclusion, the successful realization of a low-power, multi-stage decimation filter chain, along with its validation in both simulation and physical domains, marks a significant step toward practical and scalable oversampled data processing solutions. The insights and methodologies developed in this work pave the way for more sophisticated signal acquisition systems and contribute to the advancement of efficient mixed-signal interface technologies.

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