Effect of Fin Width and Fin Height on Threshold Voltage for Tripple Gate Rectangular FinFET

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***Abstract*—FinFET is a device of great importance in the semiconductor industry. Various short channel effects can be avoided by the use of finFET. The paper describes the variation of the threshold voltage with the variation in the intrinsic parameters of the finFET like fin width and fin height. Here we plot the threshold voltage of finFET in MATLAB with the minimum carrier charge density and observe the effect on threshold voltage by varying the fin width and the fin height.**

Keywords—Tripple gate rectangular finFET, MATLAB, fin height, fin width.

I. Introduction

According to Moore's law, the number of transistors per chip doubles every 18 months [1]. Our main purpose is to incorporate minimum number of transistors in a chip. This is because it reduces area, leakage current and heat dissipation. But according to Moore's law, the number of transistors in a chip is increasing day by day. One of the ways to reduce area is to scale down the size of the device. As the devices are scaled down, planar transistors have brought various degrading effects such as carrier velocity saturation, mobility degradation, hot electron effect, leakage current increment, drain induced barrier lowering, punch-through and lowering of the threshold voltage [2]. All these unwanted effects come under the short channel effect (SCE). Due to these, the devices cannot be scaled down in a rapid way. There are some possibilities which include use of silicon-on-insulator (SOI) finFET or bulk finFET. Hence the concept of multi-gate device came into existence. Recent trends show that tri-gate (TG) field-effect transistors (FETs) have been chosen as the suitable alternative for the sub-22 nm regime because it is capable of suppressing the short channel effects.

Transistor evolution from vacuum tube, followed by the BJT's having a problem of static power dissipation which can be reduced using the CMOS technology draws almost zero static power. One of the shortcomings of the CMOS technology is that the leakage current increases, on further scaling down the size of the transistors (i.e. at below 22 nm regime). To overcome this problem, SOI finFET or bulk finFET replaced planner bulk transistor. In this paper, we present the effect of threshold voltage variation with minimum carrier charge density by varying the fin width and the fin height.

Variables and constants used – Threshold voltage, minimum carrier charge density, fin width, fin height, Vd (channel potential near the drain side), acceptor and donor concentration (N_a and N_d), intrinsic carrier concentration, A_1 and A_2, Built-in potential (V_{bi}), Boltzmann constant, absolute temperature, electronic charge.

II. Structure and Operation of FinFET

A. *Structure of finFET*

The main idea of finFET and the Ultra-thin body SOI device has been given in [3].The structure of finFET comprises of a thin, vertical fin of silicon body on a substrate. The gate is wrapped around the channel from all the three sides of the channel. This structure is known as finFET because the silicon body looks like the back fin of a fish.

In a bulk MOSFET, the channel is horizontal while in case of finFET, the channel is vertical. Thus, the width of the channel is determined by the height and width of fin. The width of the transistor is given by (2*fin_ height + fin_width).

B. *Operation of finFET*

The body of the finFET is very thin. The leakage current is very low in case of finFET. The drain current increases by increasing the fin height.

We can increase the drain current by making use of parallel multiple fins connected together. The channel width is a multiple of the fin height. Thus, the overall width of the device becomes quantized. The finFET has very less dopant-induced variations. In case of the finFET, the gate wraps around the channel and the body are very thin, thus reducing the short channel effects.

III. MATLAB Simulation Set-Up

Here we have performed a MATLAB simulation showing the threshold voltage variation with the minimum carrier charge density. We observe that the threshold voltage increases with increase in charge density. We also observe that with the increase of fin width and fin height, the threshold voltage decreases.

A. Abbreviations

Some of the abbreviations used in this portion are Vt, Qth, Wfin, and Hfin. Here Vt denotes the threshold voltage, Qth indicates the minimum carrier charge density, Wfin represents fin width, and Hfin denotes fin height.

B. Units

The threshold voltage is of the order of millivolt. The fin width, the fin height, and the width of the transistor is of the order of nanometer.

C. Equations

The Threshold voltage is the minimum gate voltage required to set up a conduction path between the source and the drain. Some of the equations that we have used in the MATLAB simulation process are listed below:

$$V_t = V_{fb} - \frac{1}{(1-(A_1 - A_2))} \times \begin{pmatrix} A_1(V_{bi} + V_d) + A_2 V_{bi} \\ -V_{th} \ln\left[\frac{Q_{th} N_a}{n^2{}_i W_{fin}}\right] \end{pmatrix} \quad ..(1)$$

Where, V_{fb} is the flat band voltage. The built-in potential, V_{bi} is given by $V_{bi} = kT/q\ (\ln (N_a N_d / n_i^2))$.

Width of the transistor = (2 * fin_height) + fin_width (2)

Where A_1 and A_2 are the parameters which are the functions of natural length and channel length and it has finite values for short channel devices but for long channel devices their values are 0. V_{bi} is the built-in potential. V_d is the channel potential at the drain side. V_{th} is the thermal voltage, which is equal to kT/q, where k is the Boltzmann constant, T is the absolute temperature, and q is the electronic charge. Q_{th} is the charge density, N_a is the acceptor concentration, N_d is the donor concentration, n_i is the intrinsic carrier concentration, W_{fin} is the fin width, and H_{fin} is the fin height. Equation (1) is taken from [4].

IV. Results and Discussions

A. *Threshold voltage variation with the minimum carrier charge density*

In this paper we study the variation of threshold voltage with respect to minimum charge density by taking the constant values of acceptor and donor concentration.

From Table1, we can conclude that with the increase of charge density, the threshold voltage increases. This is further proved by the curve in Fig. 1.

Table 1: Variation of threshold voltage with charge density.

Minimum Carrier Charge Density (Qth)	Threshold Voltage (mV)
1	3.1333
2	3.1513
3	3.1619
4	3.1693
5	3.1751

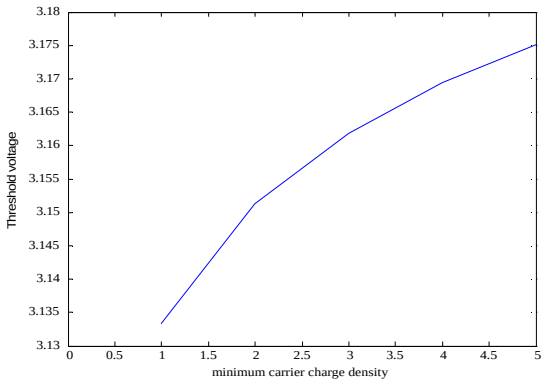

Fig. 1. Plot of V_t

From Fig 1, we can draw a conclusion that if the charge density is low, then the threshold voltage obtained will be low. It means that we need low gate voltage to turn on the device. On the other hand, subthreshold leakage will increase if we keep the threshold voltage low. On keeping threshold voltage high, we need high gate voltage to turn on the device. Thus, we have to choose optimum threshold voltage to avoid suchproblems. This can be done by adjusting the charge density in such a way that we can achieve the optimum threshold voltage.

B. *Threshold voltage variation for different values of fin width*

A very important geometrical parameter of finFET is fin width. The threshold voltage of the device has been observed in this study by varying the fin width in Table 2. From Table 2, it is clear that the value of the threshold voltage increases with the corresponding increase in the value of the charge density. If the device dimensions i.e. the fin width changes, the value of the threshold voltage also changes accordingly.

Table 2: Variation in Threshold voltage by varying the width & the Charge density.

Fin Width (nm)	Charge Density (Qth)	Threshold Voltage(mV)
0.1	1	3.1513
	2	3.1693
	3	3.1799
	4	3.1874
	5	3.1932
0.2	1	3.1333
	2	3.1513
	3	3.1619
	4	3.1693
	5	3.1751
0.3	1	3.1228
	2	3.1408
	3	3.1513
	4	3.1588
	5	3.1646

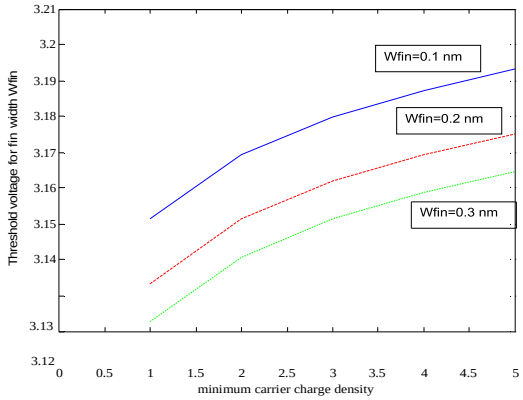

Fig. 2. Plot of V_t vs. Q_{th} by varying Fin Width

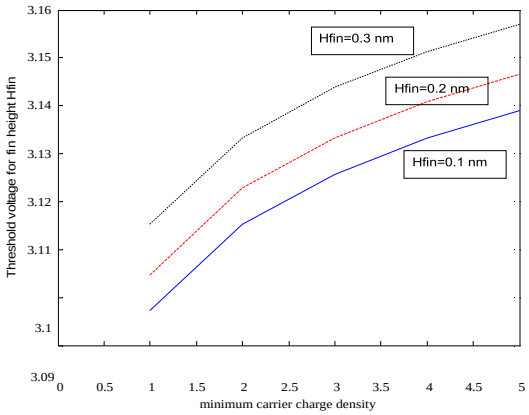

Fig. 3. Plot of V_t vs. Q_{th} by varying fin height

The curve, which is obtained from MATLAB simulation, is given in Fig. 2.

From the curve in Fig. 2, we can draw a conclusion that a change in the dimension of the device (i.e. a change in the fin width) affects the threshold voltage of the device. The threshold voltage of the device is inversely proportional to the fin width of the device.

C. *Threshold Voltage variation for different values of fin height*

We know that the width of the transistor = (2 * fin_height + fin_width). From the concept of general mathematics, if the width of the transistor is fixed and the device dimension (i.e. the fin height) increases or decreases, then the threshold voltage increases or decreases respectively. This is exactly, what is observed from the Table 3, where we have considered the width of the transistor to be 1nm.

Table 3: Different Threshold voltages with respect to varying height & Charge density with fixed Width of the Transistor

Fin Height (nm)	Minimum carrier charge density (Qth)	Threshold Voltage (mV)
0.1	1	3.0973
	2	3.1153
	3	3.1258
	4	3.1333
	5	3.1391
0.2	1	3.1047
	2	3.1228
	3	3.1333
	4	3.1408
	5	3.1466
0.3	1	3.1153
	2	3.1333
	3	3.1438
	4	3.1513
	5	3.1571

Whatever we have discussed before prove to be true from the values of the threshold voltage given in Table 3. The curves are provided in Fig. 3 to make it easier for the readers to understand the fact more clearly.

From (2), it is obvious that if both the width of the transistor and the fin_height increase, then the threshold voltage decreases and vice-versa. Table 4 proves the above-mentioned fact.

From Table 4, we can observe that the threshold voltage decreases with the corresponding increase in the width of the transistor and the fin_height. This is because as the width of the transistor and the fin_height increase, the fin width also increases, resulting in decrease of the threshold voltage. This can be clarified further by the curve shown in Fig. 4.

Table 4: Different Threshold voltages with respect to varying height & Charge density with varying Width of the Transistor

Width of the transistor (nm)	Fin Height (nm)	Minimum carrier charge density (Qth)	Threshold Voltage (mV)
1	0.1	1	3.0973
		2	3.1153
		3	3.1258
		4	3.1333
		5	3.1391
2	0.2	1	3.0792
		2	3.0973
		3	3.1078
		4	3.1153
		5	3.1211
3	0.3	1	3.0687
		2	3.0867
		3	3.0973
		4	3.1047
		5	3.1105

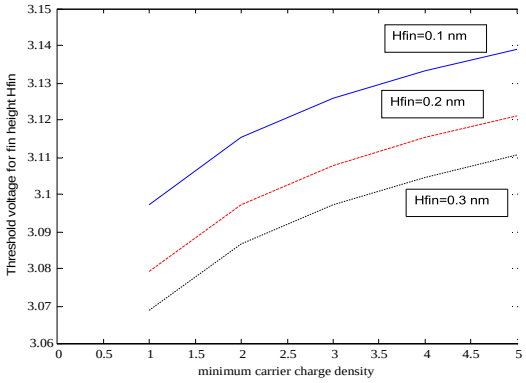

Fig. 4. Plot of V_t vs. Q_{th} by varying fin_height

Now, it becomes easier to understand about the threshold voltage variation with the corresponding change in the width of the transistor and the fin_height.

V. Conclusion

In this paper, MATLAB simulation of threshold voltage is carried out. We observe and analyze the variation of threshold voltage with different values of fin_width, and fin_ heights. Short channel effect is less in rectangular finFET.

References

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